P/N	SH	REV
610-20198-01	1	1.0

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES. .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.
   ~~C. FILL ALL VIAS ON PASTE WITH COPPER PLATING OR NON-CONDUCTIVE EPOXY; DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. FOR EPOXY FILL, OVERPLATE WITH COPPER, .005 [.0002] MINIMUM AND THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.~~
   ~~D. FILL ALL BURIED VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .005 [.0002] MINIMUM THICKNESS. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.~~

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR RED.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:
   A. FINAL FINISH ON ALL EXPOSED CONDUCTORS SHALL BE 2 MICROINCH GOLD IMMERSION.
   B.FINAL FINISH ON ALL THE GOLD FINGER BEVEL DEFAULT VALUE : 20 DEGREES , DEPTH : 11.8 MILS. FINAL FINISH ON ALL EXPOSED GOLD FINGER SHALL BE 30 MICROINCH HARD GOLD PLATED.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

REVISIONS

ECO NO.	REV	DATE	DESCRIPTION	DRAWN	CHECKED	APPROVED
XJZH#226	1.0	08/18/23	INITIAL RELEASE	LIKZ	XJZH	LIKZ

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
•	7.87	+1.97/-7.87	PLATED	212
⊘	137.8	+2.95/-2.95	NON-PLATED	1

STACKUP

1OZ	COPPER PLATING		LAYER 1 - TOP
	PREPREG		
.5OZ	COPPER		LAYER 2
	PREPREG		
.5OZ	COPPER		LAYER 3
	PREPREG		
1OZ	COPPER PLATING		LAYER 4 - BOTTOM

TOTAL:0.80MM+/-0.08M

50OHMS 7MIL@TOP LAYER

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES WITH METRIC IN BRACKETS
.XXX ±.005 [±.064] .XX ±.01 [±.13] ANGLES ±.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN JYUN	08/18/23
ENGINEER LYAN	08/18/23
CHECKER LYAN	08/18/23
QA N/A	N/A
PROJ. ENG. N/A	N/A

Infineon Technologies AG
IFAG MUC Am Campeon 1-15
85579 NEUBIBERG - GERMANY

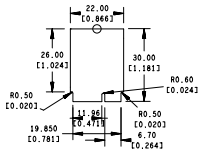
TITLE: PCB FABRICATION, CYW920829B0M2P4XXI100

SIZE	CAGE CODE	P/N
D	-	610-20198-01

SCALE	SHEET	REV
1/1	1 OF 2	1.0

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

REVISIONS						
ECO NO.	REV	DATE	DESCRIPTION	DRAWN	CHECKED	APPROVED
XJZH#226	1.0	08/18/23	INITIAL RELEASE	LIKZ	XJZH	LIKZ



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SIZE	CAGE CODE	P/N
D	-	610-20198-01
SCALE 1/1		SHEET 2 OF 2 | REV 1.0

COMPUTER GENERATED DRAWING
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